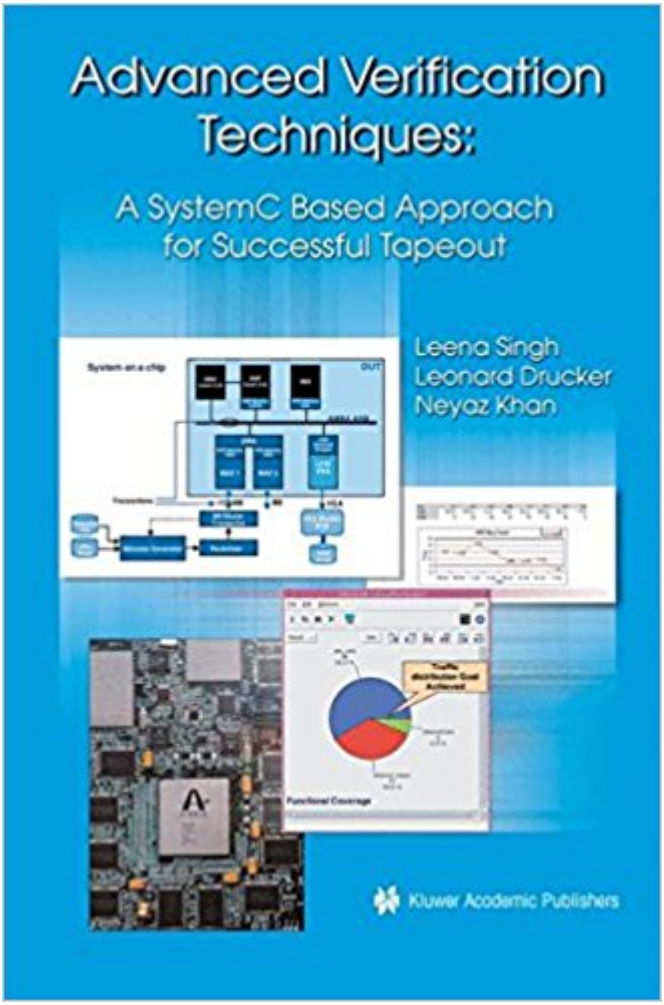
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Advanced Verification Techniques: A SystemC Based Approach For Successful Tapeout



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Synopsis

"As chip size and complexity continues to grow exponentially, the challenges of functional verification are becoming a critical issue in the electronics industry. It is now commonly heard that logical errors missed during functional verification are the most common cause of chip re-spins, and that the costs associated with functional verification are now outweighing the costs of chip design. To cope with these challenges engineers are increasingly relying on new design and verification methodologies and languages.Ã Â Transaction-based design and verification, constrained random stimulus generation, functional coverage analysis, and assertion-based verification are all techniques that advanced design and verification teams routinely use today. Engineers are also increasingly turning to design and verification models based on C/C++ and SystemC in order to build more abstract, higher performance hardware and software models and to escape the limitations of RTL HDLs. This new book, Advanced Verification Techniques,Ã Â provides specific guidance for these advanced verification techniques. The book includes realistic examples and shows how SystemC and SCV can be applied to a variety of advanced design and verification tasks."Ã Â - Stuart Swan

Book Information

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"As chip size and complexity continue to grow exponentially, the challenges of functional verification are becoming a critical issue in the electronics industry. It is now commonly heard that logical errors missed during functional verification are the most common cause of chip re-spins, and that the costs associated with functional verification are now outweighing the costs of chip design. To cope with these challenges engineers are increasingly relying on new design and verification methodologies and languages. Transaction-based design and verification, constrained random stimulus generation, functional coverage analysis, and assertion-based verification are all techniques that advanced design and verification teams routinely use today. Engineers are also increasingly turning to design and verification models based on C/C++ and SystemC in order to build more abstract, higher performance hardware and software models and to escape the limitations of RTL HDLs. This new book, Advanced Verification Techniques, provides specific guidance for these advanced verification techniques. The book includes realistic examples and shows how SystemC and SCV can be applied to a variety of advanced design and verification tasks." (Stuart Swan)

This book is very poorly written. I don’t know how it got past editors, but it is full of grammatical errors (about 5-10 per page), and unfortunately the errors get in the way of reading the material. Explanations are also poor, and knowledge is assumed without prior explanation. They even describe files that are not in the book itself, but are only visible from a web site! Some sentences make no sense at all. The text sometimes refers to the wrong figures. However, they do try and be comprehensive, and cover a huge amount of practical material. It is short on theory or any justification for many of the assertions they make. Some almost throw-away comments indicate they know their stuff well, but this book is very much for advanced practitioners only. I can’t help feeling that some of it was directly transcribed from notes they made to themselves when they were bored in meetings. They tried to use previous projects as real-world examples, but the examples are so complex that you can’t follow them unless you have expertise in various areas already (e.g. OC-48, OC-192, ATM, etc).

Anyone with any experience running simulation will not find anything in this book besides frustration. System C examples are woefully incomplete, without even one useful example. The authors attempt to describe semi advanced techniques without even laying out the basics of instantiating a complete test bench structure properly. About the only thing useful are flow charts of a proper testbench.

This book is not good at all. Poorly written and incomplete and typos in examples/illustrations. Most of the examples are written in test Builder even though the book says SystemC Based Approach. Many of the concepts in verification methodology can be found in other verification books and this book adds very little value.

Practical book with some good examples we could use in our training. It will be more helpful if the examples are converted to latest versions of SystemC.

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